



RBX1600 Hardware Theory of Operation and Programming Guide

***StreetFire Sound Labs
Version 1.01***

Document History

<i>Date</i>	<i>Description</i>
08/10/04	Preliminary Release
08/12/04	Added copy right, fixed LED headers and changed RS-232 Cable spec.
08/15/04	Changed title of document and changed Section 3 Title to reduce confusion

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1 Introduction

The RBX1600 is a microprocessor based consumer electronic device for controlling up to four Sony MegaStorage CD Players. Integrated software allows the user to catalog, play and managed up to 1600 CD-Audio discs via a PC based software client. The RBX1600 connects to the users home network environment via a high performance 10/100 Ethernet interface.

1.1 System Features

The RBX1600 has a the following key hardware features:

- 1 StreetRacer CPU Card with 64MB RAM and 64MB Flash.
- 1 RS-232 interface with hardware flow control on a mail DB-9 connector.
- 1 10/100 Ethernet port on a RJ-45 connector.
- 4 Digital audio input ports on TOSLink optical receiver.
- 1 Digital audio output port on a TOSLink optical transmitter.
- 1 Analog audio output port on a two channel RCA connector.
- 6 Bi-directional Sony SLink control channels on 3.5mm phone jacks.
- 1 Sony compatible infrared input port.
- 1 USB 1.1 device interface on USB device connector.
- 1 Front panel power control switch
- 1 Front panel power status LED.
- 4 Front panel channel status LED.
- 1 12VDC external power supply.

1.2 System Overview

Internally the RBX1600 is composed of two major components: a StreetRacer CPU Card and an Application Board.

The StreetRacer CPU Card is a single board designed to plug into a application or personality board via a 168 pin DIMM socket. The initial version of the StreetRacer CPU Card uses a 400MHz Intel PXA255 XScale microprocessor based on the v.5TE ARM core with 64M of 100MHz SDRAM, 64M NOR flash and a 400K gate SpartanIIe FPGA. The unique architecture of the StreetRacer CPU Card allows the DIMM connector to be mapped and programmed via the FPGA.

The Application Board provides the major external interfaces for the RBX1600 system including the Digital Audio Control subsystem, the Sony SLINK device interface subsystem, and the 10/100 Ethernet subsystem. Additionally, the front panel hardware

interface, the RS-232 interface and then device USB 1.1 interface are provided by the Application Board. The StreetRacer CPU Card is hosted by the Application Board via a 168 pin DIMM socket.

1.3 What's Next

The remainder of this document provides a integrated theory of operation for the RBX1600 system. Section 2 provides detailed look at the all hardware subsystems. Section 3 provides programming interface details for all RBX1600 specific peripherals and interfaces. Appendix A provides references to non-StreetFire Sound Labs documentation.

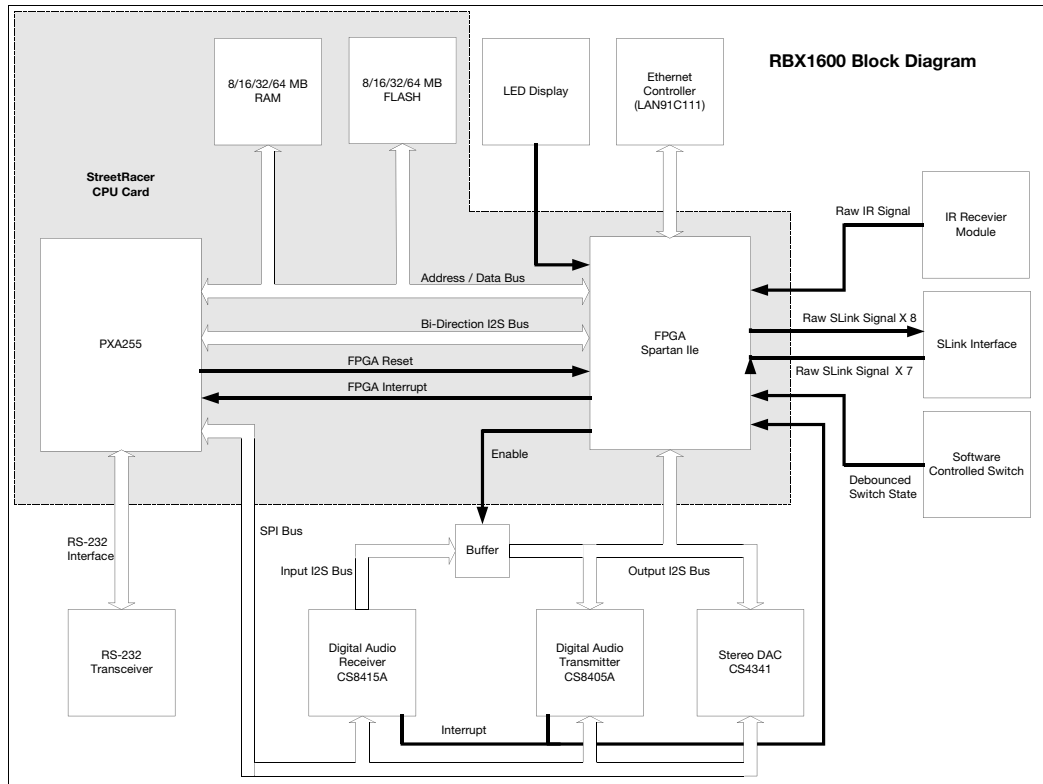


Figure 1 RBX1600 Block Diagram

2 Hardware Description

This section describes the RBX1600 hardware platform and all of its subsystems:

- Section 2.1 covers the RBX1600 Application Board
- Section 2.2 covers the StreetRacer CPU Card.

While information in this chapter and Chapter <<????> provides enough detail to understand the operation and the RBX1600; it is strongly recommended that the user reference the original manufacturer data sheets for all devices incorporated into the RBX1600.

2.1 RBX1600 Application Board

The RBX1600 Application Board hosts the external peripherals which provide the system its personality. The application board is composed of six major subsystems:

- A variable voltage DC power input controller.
- A 10/100 Ethernet MAC controller with integrated PHY bridged.
- A 8 Channel SLINK controller with 7 bi-directional Control-AI/II ports, 1 output only Control-S port and 1 IR input only port.
- A 3 chip digital audio controller supporting 7 digital audio inputs, 1 digital audio output and 1 analog audio output under microprocessor control via a SPI bus and supporting a single bidirectional I2S bus for digital audio recording and playback.
- A front panel controller with 5 LED outputs and 1 mechanical switch input.
- A USB Device interface.
- A RS-232 interface with hardware flow control.

2.1.1 Variable Voltage DC Power Input Subsystem

The power input subsystem provides all core voltages to the system. Input power may be sourced from a regulated or unregulated external power brick. The input power must be provided on a center-positive jack with an inside diameter of 0.080" and an outside diameter of .218". For a regulated power supply the input voltage may range from +7.0V to +18V DC. For an unregulated power supply the input voltage may range between +9V to +12V. The minimum power rating is 9W.

The input power voltage is converted and regulated to 3.3V and 5V via two Linear Technology's LT1765 Monolithic 3A, 1.25MHz Step-Down Switch Regulators.

The output power can be checked via the following test points:

Test Point	Value
TP1	+3.3V
TP4	+5.0V

<i>Test Point</i>	<i>Value</i>
TP5	Ground

Table 1 Voltage Test Points

<<GET MARIO TO DESCRIBE THE LED POWER MONITORING SCHEME AGAIN>>

The power input system provide 3.3V to the StreetRacer CPU via the DIMM socket.

2.1.2 10/100 Ethernet Subsystem

The Ethernet subsystem uses a SMC, LAN91C111 “10/100 Non-PCI Ethernet Single Chip MAC + PHY” controller combined with a Tyco, 5-1605706-1 “Integrated Magnetic 1X1 Single Port Modular Jack” to provide a high performance 10/100 Ethernet interface. An ATMEL AT93C46 “3-wire Serial EEPROM” connected to the LAN91C11 Serial EEPROM interface to provide 1024 bits of persistent configuration storage for the power-on MAC address.

Ethernet interface status is provides by integrated LED on the RJ-45 jack. By default the yellow LED indicates the presence of the LINK and the green LED indicates the presence of Ethernet traffic.

The LAN91C111 is connected to the StreetRacer CPU Card via the 168 pin DIMM socket in a hybrid asynchronous 32-bit bus mode with an interrupt signal also routed to the DIMM socket.

Headers J11 and J12 provide access to the LAN91C111 address/data bus and all control signals.

<i>Signal</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal</i>
D0	1	2	D1
D2	3	4	D3
D4	5	6	D5
D6	7	8	D7
D8	9	10	D9
D10	11	12	D11
D12	13	14	D13
D14	15	16	D15
D16	17	18	D17
D18	19	20	D19
D20	21	22	D21
D22	23	24	D23
D24	25	26	D25
D26	27	28	D27
D28	29	30	D29

<i>Signal</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal</i>
D30	31	32	D31
D32	33	34	A1
A2	35	36	A3
GND	37	38	GND
GND	39	40	GND

Table 2 Ethernet Address and Data Bus Header

<i>Signal</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal</i>
BE0#	1	2	BE1#
BE2#	3	4	BE3#
RD#	5	6	WR#
ADS#	7	8	ARDY
INTR#	9	10	RESET
W/R#	11	12	RDYRTN#
LDEV#	13	14	DATACS#
LCK	15	16	CYCLE#
VLBUS#	17	18	GND
GND	19	20	GND

Table 3 Ethernet Control Signal Header

2.1.3 Sony SLINK Subsystem

The Sony SLINK subsystem uses a custom 8 channel SLINK controller implemented the StreetRacer CPU Card FPGA by StreetFire Sound Labs. SLINK is 5V active low, return to high variable bit rate serial protocol developed by Sony.

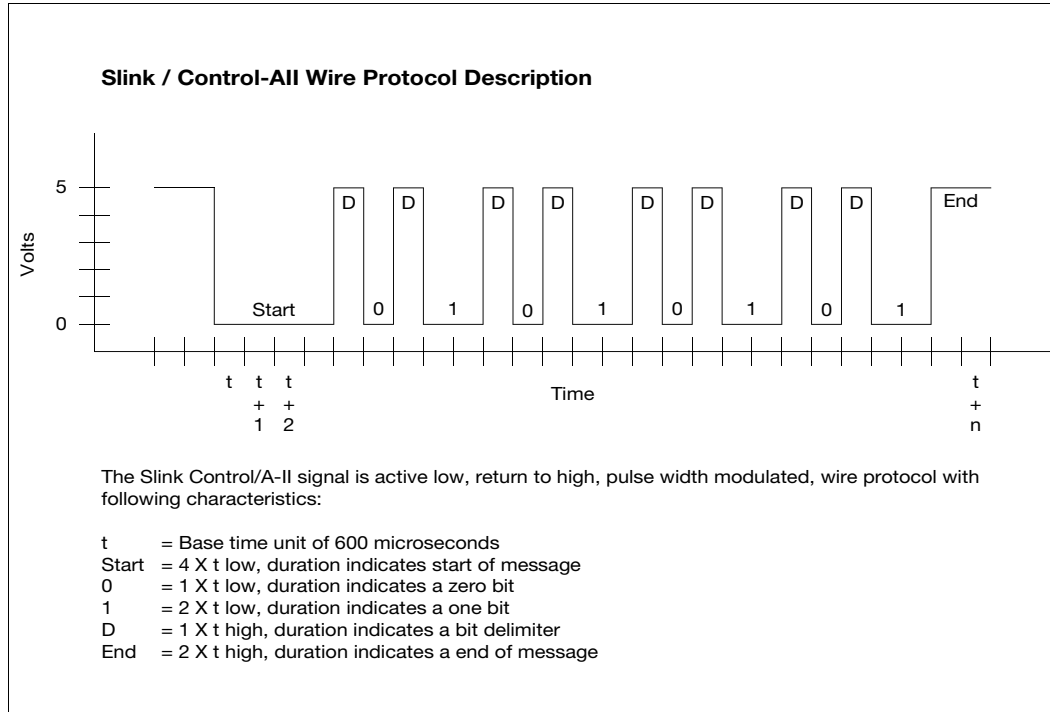


Figure 2 SLINK Protocol Description

The RBX1600 provides with 7 bi-directional Control-AI/II ports, 1 output only Control-S port and 1 IR input only port, all which use the same basic protocol.

The 8 channels are connected to the StreetRacer CPU Card and FPGA via the 168 pin DIMM socket.

Header J5 provide access to the 7 bi-direction Control-AI/II ports and the single Control-S port. U10 provides the IR input port.

Signal	Pin	Pin	Signal
GND	1	2	SLINK0
GND	3	4	SLINK1
GND	5	6	SLINK2
GND	7	8	SLINK3
GND	9	10	SLINK4
GND	11	12	SLINK5
GND	13	14	SLINK6
GND	15	16	SLINK7

Table 4 SLINK Signal Header

2.1.4 Digital Audio Subsystem

The Digital Audio Subsystem is a 3 chip digital audio controller supporting 4 digital audio inputs, 1 digital audio output and 1 analog audio output under microprocessor control via a SPI bus and supporting a single bidirectional I2S bus for digital audio recording and playback. The audio subsystem is implemented using the following Cirrus Logic chips:

- CS8415A 96kHz Digital Audio Interface Receiver
- CS8405A 96kHz Digital Audio Interface Transmitter
- CS4341 24-bit, 96kHz Stereo DAC with Volume Control

2.1.4.1 External Connections

Digital audio is input via TOSLink optical receivers OPT1, OPT2, OPT3 and OPT4. The TOSLink receiver output are connected to the CS8415A's 7:1 receiver multiplexer.

<i>TOSLink</i>	<i>CS8415A Port</i>
OPT1	RXP3
OPT2	RXP2
OPT3	RXP1
OPT4	RXP0

Table 5 TOSLink Connector Positions

Digital audio is output via a single TOSLink optical transmitter OPT5. The TOSLink transmitter input is connected to the CS8405A TXP line.

Digital audio is converted into analog by the CS4341 and the analog signal is output via a 2 channel RCA connector J6.

2.1.4.2 Microprocessor Control

The CS8415A, CS8405A and CS4341 are controlled by the StreetRacer CPU Card via a Serial Peripheral Interface (SPI) bus with external 3 chip selects. The Cirrus chip's SPI clock, receive and transmit lines are connected to the direct mapped PXA255 NSSP port. The CS8415A and CS8405A are capable of generating interrupts which are routed to StreetRacer CPU Card FPGA and available in a FPGA peripheral block.

<i>Signal</i>	<i>PXA255</i>
CS8415A CS	GPIO_2
CS8405A CS	GPIO_3
CS4341 CS	GPIO_82
CCLK	NSSP_CLK
CDIN	NSSP_TX
CDOUT	NSSP_RX

Table 6 SPI Interface Pins

2.1.4.3 I2S Digital Audio Bus

The digital audio controller provides a bi-directional I2S bus for record and playback of audio data. The I2S bus connects the CS8415A, CS8405A, CS4341 and StreetRacer CPU Card FPGA. The FPGA is connected to the PXA255 I2S peripheral port.

The bus operates in three mode: Normal, Record, and Playback. The bus mode is controlled via a FPGA peripheral block.

<i>Mode</i>	<i>Description</i>
Normal	The CS8415A IS2 output is routed to the CS8405A and CS4341 I2S inputs.
Record	The CS8415A I2S output is also available via the PXA255 IS2 port.
Playback	The CS8415A is isolated and the PXA255 I2S port the the source of audio data for the CS8405A and the CS4341.

Table 7 I2S Bus Routing

The Digital Audio subsystem side of the I2S bus is available via header J10. For more information about this I2S bus see the appropriate Cirrus documentation.

<i>Pin</i>	<i>Signal</i>	<i>Description</i>
1	MCLK	Master Clock
2	SDATA	Serial Bit Data
3	SCLK	Serial Bit Clock
4	LRCLK	Left/Right Clock
5	GND	N/A
6	GND	N/A

Table 8 I2S Header

NOTE: Depending on the FPGA configuration the PXA255 side of the I2S bus may be available on the FPGA I/O header J8.

2.1.5 Front Panel Subsystem

The Front Panel subsystem provides five independently accessible LED outputs and one mechanical switch input. Access to the LED outputs and the switch input is via a custom controller implemented in the StreetRacer CPU Card FPGA.

2.1.6 USB Device Interface

The USB Device subsystem provides a USB 1.0 device interface delivery on a standard USB Device connector, J4. The connector is wires to the StreetRacer CPU Card via the 168 pin DIMM socket and mapped directly to the PXA255 USB peripheral port.

The state of the USB connection is presented on the DIMM socket at pin 151 and PXA255 GPIO4. A logic zero indicated the USB device in connected.

The PXA255 GPIO14 can be used to force the remote USB host to disconnect. A logic

one on GPIO14 will force the remote USB host to disconnect.

2.1.7 RS-232 Interface

The RS-232 subsystem provide access to the industry standard UART with hardware flow control on a male DB-9 connector. The connector wired 168 pin DIMM socket and mapped directly to the PXA255 Full Function UART peripheral port. Only RTS/CTS is provided, no modem control signal are connected. A standard female-female DB-9 null modem cable maybe used to connect the serial port to a PC.

<i>DB-9 Pin</i>	<i>Description</i>
1	NC
2	RX
3	TX
4	NC
5	GND
6	NC
7	RTS
8	CTS
9	NC

Table 9 RS-232 DB-9 Pin out

2.1.8 RBX1600 Card Edge Definition

The RBX1600 edge is designed to mate with the StreetRacer CPU Card. The RBX1600 has a Molex's 87609-0059, "DIMM 8-Byte, 168 Circuit" connector. The following table presents the RBX1600 card definition which defines the interface between the RBX1600 hosted peripherals and the CPU Card.

<i>RBX1600</i>	<i>StreetRacer</i>	<i>Pin</i>	<i>Pin</i>	<i>StreetRacer</i>	<i>RBX1600</i>
GND	GND	1	85	EB85	ETH_A1
ETH_D0	EB2	2	86	EB86	ETH_A2
ETH_D1	EB3	3	87	EB87	ETH_A3
+3.3V	+3.3V	4	88	GND	GND
ETH_D2	EB5	5	89	EB89	SW_1
ETH_D3	EB6	6	90	EB90	DBG2
ETH_D4	EB7	7	91	+3.3V	+3.3V
GND	GND	8	92	EB92	DBG3
ETH_D5	EB9	9	93	EB93	DBG4
ETH_D6	EB10	10	94	EB94	DBG5
ETH_D7	EB11	11	95	GND	GND
GND	GND	12	96	EB96	DBG6

<i>RBX1600</i>	<i>StreetRacer</i>	<i>Pin</i>	<i>Pin</i>	<i>StreetRacer</i>	<i>RBX1600</i>
I2S_MCLK	GCK3	13	97	VCC_BANK0	+3.3V
GND	GND	14	98	EB98	DBG7
ETH_D8	EB15	15	99	GND	GND
+3.3V	VCC_BANK7	16	100	EB100	ETH_BE0_N
ETH_D9	EB17	17	101	EB101	ETH_BE1_N
ETH_D10	EB18	18	102	+3.3V	+3.3V
GND	GND	19	103	EB103	ETH_BE2_N
ETH_D11	EB20	20	104	EB104	ETH_BE3_N
ETH_D12	EB21	21	105	GND	GND
+3.3V	+3.3V	22	106	EB106	ETH_VLBUS_N
ETH_D13	EB23	23	107	EB107	ETH_CS
ETH_D14	EB24	24	108	+3.3V	+3.3V
GND	GND	25	109	EB109	ETH_RD_N
ETH_D15	EB26	26	110	EB110	ETH_WR_N
ETH_D16	EB27	27	111	GND	GND
+3.3V	+3.3V	28	112	EB112	ETH_ADS_N
ETH_D17	EB29	29	113	EB113	ETH_LCLK
ETH_D18	EB30	30	114	+3.3V	+3.3V
GND	GND	31	115	EB115	ETH_DATACS_N
ETH_D19	EB32	32	116	GND	GND
+3.3V	+3.3V	33	117	EB117	ETH_W/R_N
ETH_D20	EB34	34	118	GND	GND
GND	GND	35	119	EB119	ETH_CYCLE_N
ETH_D21	EB36	36	120	+3.3V	+3.3V
+3.3V	+3.3V	37	121	VCC_BANK7	+3.3V
ETH_D22	EB38	38	122	GND	GND
+3.3V	+3.3V	39	123	EB123	ETH_RDYRTN_N
ETH_D23	EB40	40	124	EB124	ETH_IOWAIT
ETH_D24	EB41	41	125	+3.3V	+3.3V
GND	GND	42	126	EB126	ETH_LDEV_N
ETH_D25	EB43	43	127	EB127	ETH_INT
ETH_D26	EB44	44	128	GND	GND
GND	GND	45	129	EB129	LED_0
ETH_D27	EB46	46	130	EB130	LED_1
ETH_D28	EB47	47	131	+3.3V	+3.3V
+3.3V	+3.3V	48	132	EB132	LED_2

<i>RBX1600</i>	<i>StreetRacer</i>	<i>Pin</i>	<i>Pin</i>	<i>StreetRacer</i>	<i>RBX1600</i>
ETH_D29	EB49	49	133	EB133	ETH_RESET
ETH_D30	EB50	50	134	GND	GND
GND	GND	51	135	EB135	LED_3
ETH_D31	EB52	52	136	EB136	LED_4
+3.3V	VCC_BANK6	53	137	VCC_BANK6	+3.3V
SL_TX_0	EB54	54	138	GND	
SL_RX_0	EB55	55	139	EB139	DA_INT_8415A
GND	GND	56	140	EB140	DA_INT_8405A
SL_TX_1	EB57	57	141	EB141	I2S_MCLK
SL_RX_1	EB58	58	142	+3.3V	+3.3V
SL_TX_2	EB59	59	143	EB143	I2S_LRCLK
+3.3V	+3.3V	60	144	EB144	I2S_SDATA
SL_RX_2	EB61	61	145	EB145	I2S_SCLK
SL_TX_3	EB62	62	146	GND	+3.3V
SL_RX_3	EB63	63	147	GCK1	I2S_SCLK
GND	GND	64	148	nRESET_OUT	SYS_RESET
UNUSED GPIO_0	GPIO0	65	149	GPIO1	UNUSED GPIO_1
SPI_CS0	GPIO2	66	150	+3.3V	+3.3V
SPI_CS1	GPIO3	67	151	GPIO4	USB_DWAKE
+3.3V	GND	68	152	IRRXD/GPIO46	UNUSED GPIO_46
UNUSED GPIO_7	IRTXD/GPIO47	69	153	GND	GND
UNUSED I2C_SCL	SCL	70	154	SDA	UNUSED I2C_SDA
GND	GND	71	155	UDCP	UDCP
UDCN	UDCN	72	156	+3.3V	+3.3V
SPI_CS2	NSSPSFRM/GPIO82	73	157	NSSPCLK/GPIO81	SPI_CLK
+3.3V	+3.3V	74	158	NSSPRXD/GPIO84	SPI_RXD
SPI_TXD	NSSPTXD/GPIO83	75	159	GND	GND
SL_TX_4	SSPTXD/GPIO25	76	160	SSPRXD/GPIO26	IR_TX
GND	GND	77	161	SSPSFRM/GPIO24	IR_RX
SL_RX_4	SSPEXTCLK/GPIO27	78	162	SSPSCLK/GPIO23	DAI_ENABLE
SL_TX_5	FFRI/GPIO38	79	163	+3.3V	+3.3V
SL_RX_5	FFDSR/GPIO37	80	164	FFDCD/GPIO36	SL_TX_6
+3.3V	+3.3V	81	165	FFDTR/GPIO40	SL_RX_6
FF_RTS	FFRTS/GPIO41	82	166	GND	GND
FF_TXD	FFTXD/GPIO39	83	167	FFCTS/GPIO35	FF_CTS
GND	GND	84	168	FFRXD/GPIO26	FF_RXD

Table 10 RBX1600 Card Edge Pin out

2.1.9 Miscellaneous Stuff

There are two addition headers on the RBX1600 application board: J8 and J9. J8 provides access to a debug port for the FPGA. Please contact StreetFire Sound Labs to determine the signals available on this port as it varies based on the FPGA configuration.

<i>Pin</i>	<i>Signal</i>
1	NC
2	EB90
3	EB92
4	EB93
5	EB94
6	EB96
7	EB98
8	GND

Table 11 FPGA Debug Port Header

J9 provides access to the PXA255 Standard UART, I2C bus as well as several PXA255 GPIO pins.

<i>Pin</i>	<i>Signal</i>
1	+5V
2	I2C SCL
3	I2C SDA
4	GPIO_0
5	GPIO_1
6	GPIO_47/ST_TXD
7	GPIO_46/ST_RXD

Table 12 CPU Debug Header

2.2 StreetRacer CPU Card

The StreetRacer CPU Card powers the RBX1600 system with a 400mHZ Intel PXA255 XScale processor, 64MB of 100mHZ SDRAM and 64MB of NOR type flash. A Xilinx SpartanIIe FPGA drives a reconfigurable 168 pin DIMM card edge connector with a field upgradeable companion chip interface. The companion chip interface defines 32 4K custom peripheral blocks with a common interrupt controller and chip configuration interface.

The StreetRacer CPU Card exposes via the DIMM card edge or on board headers, the following peripherals from the PXA255:

- LCD Controller.

- Network Synchronous Serial Port Controller.
- Synchronous Serial Port.
- Blue Tooth UART.
- Full Function UART.
- Standard UART.
- JTAG Interface
- Compact Flash Slot.
- 7 General purpose I/O pins.

2.2.1 Power and Reset Subsystem

The Power and Reset subsystem provides core voltages the CPU card. 3.3VDC input power to the card is provided on pin present on 168 pin DIMM card edge. The input current must be at least 1600mA with a ramp time for ground to 3.3VDC of less than 2ms with no voltage dips. Reference Xilinx XAPP450 and XAPP451 for exact requirements.

Two on-board voltages are created:

550mA, 1.5VDC PXA255 core voltage is created by a Linear Technologies, LTC1878 “High Efficiency Monolithic Synchronous Step-Down Regulator”.

550mA, 1.8VDC FPGA core voltage is created by a National Semi Conduction, LM1086CSX “1.5A Low Dropout Regulator”

The PXA255 is held in reset for 250ms after the 3.3VDC input power has reached 3.08VDC by a Microchip, TC1270TERC “4-Pin uP Reset Monitor”. <<????>>ms after the PXA255 is released from reset, the processor releases the rest of the system from hardware reset. The hardware reset is distributed to the application board via RESET_OUT_N of the edge connector.

SW1 provide a manual hardware reset capability.

The Power subsystem allows the FPGA banks 0, 6 and 7 to be powered independently from the the rest of the StreetFire CPU Card. These independent bank voltages are applied to the FGPA after the 1.8VDC core input voltage is has reached <<check this>> and are provided to the card via card edge pins VCC_BANK0, VCC_BANK6 and VCC_BANK7.

2.2.2 Memory Subsystem

The Memory Subsystem of the StreetRacer CPU card provides 16, 32 or 64 megabytes of SDRAM and 16, 32 or 64 megabytes of Flash memory. This actual amount is configured during manufacturing.

2.2.2.1 SDRAM

SDRAM memory is wired in a 2 chip 32 bit wide, configuration using Micron MT46LC16M16A2TG-75 or similar SDRAM chips. The SDRAM is located on the PXA255 SRDAM Bank 0 and uses the nSDCS_0, nSDCKE_1 and nSDCLK_1 for access and clock control.

Memory size configuration is accomplished using 0 ohm resistors as jumpers.

<i>Memory Size</i>		<i>R29, R98, R100</i>	<i>R30, 99</i>
16MB	64MBit X2	DNI	0.0 ohm
32MB	128Mbit X 2	DNI	0.0 ohm
64MB	256Mbit X2	0.0 ohm	DNI

Table 13 SDRAM Board Assembly Configuration

2.2.2.2 Flash

Flash memory is wired in 1 or 2 chip, 16 bit or 32 bit wide configuration. Both TSOP and BGA footprints are available. A variety of Intel J3 and K3 type flash chips may be used: RC/E28F640J3A, RC/E28F128J3A or RC28F256K3C.

0 ohm configuration resistors select Intel flash types J3 Asynchronous, K3 Asynchronous or K3 Synchronous. Flash memory is located on the PXA255 Static Bank 0 and uses nCS0, nSDCLK0 for access and clock. A wire-or version of the flash write status, STS is available of the PXA255 GPIO7. Flash memory is used to boot the board.

Memory size configuration is accomplished using 0 ohm resistors as jumpers.

<i>Resistor</i>	<i>J3</i>	<i>K3</i>
R31	0 ohm	DNI
R39	0 ohm	DNI
R37	DNI	0 ohm
R43	DNI	0 ohm
R38	10K	DNI
R44	10K	DNI
R36	DNI	0 ohm
R41	DNI	0 ohm
R22	DNI	10K
R40	DNI	0 ohm

Table 14 Flash Board Assembly Size Configuration

<i>Resistor</i>	<i>J3-Async</i>	<i>K3-Async</i>	<i>K3-Sync</i>
R42	DNI	DNI	0 ohm
R45	DNI	DNI	0 ohm
R67	DNI	10K	DNI
R43	DNI	10K	DNI

Table 15 Flash Board Assembly Type Configuration

2.2.2.3 Memory Map

<i>Address</i>	<i>Size</i>	<i>Description</i>
0xA4000000	1472M	Reserved
0xA0000000	64M	SDRAM Bank
0x4C000000	1344M	Reserved
0x48000000	64M	PXA255 Memory Controller
0x44000000	64M	PXA255 LCD
0x40000000	64M	PXA255 Peripherals
0x30000000	256M	Reserved
0x20000000	256M	Compact Flash Slot
0x18000000	128M	Reserved
0x14000000	64M	FPGA Peripheral Blocks 16 - 31
0x10000000	64M	FPGA Peripheral Blocks 0 - 15
0x0C000000	64M	Reserved, FPGA
0x08000000	64M	Reserved, FPGA
0x04000000	64M	Reserved, FPGA
0x00000000	64M	Flash Memory

Table 16 Memory Map

2.2.3 PXA255 Boot Configuration

The StreetRacer CPU card can be configured to boot from a variety of memory located in the PXA255 Static Bank 0. See Intel's PXA255 Processor Developer's Manual for additional information.

<i>Boot From</i>	<i>R95</i>	<i>R94</i>	<i>R93</i>	<i>R92</i>	<i>R91</i>	<i>R90</i>
Async 32 Bit ROM	100K	DNI	100K	DNI	100K	DNI
Async 16 Bit ROM	100K	DNI	100K	DNI	DNI	100K
Reserved	100K	DNI	DNI	100K	100K	DNI
Reserved	100K	DNI	DNI	100K	DNI	100K
16/32 Bit Sync Mask ROM 32 or 64M bit each	DNI	100K	100K	DNI	100K	DNI

<i>Boot From</i>	<i>R95</i>	<i>R94</i>	<i>R93</i>	<i>R92</i>	<i>R91</i>	<i>R90</i>
16 Bit Sync Mask ROM	DNI	100K	100K	DNI	DNI	100K
16 Bit Sync Mask ROM 64M Bit each	DNI	100K	DNI	100K	100K	DNI
16 Bit Sync Mask ROM 32M Bit each	DNI	100K	DNI	100K	DNI	100K

Table 17 CPU Boot Assembly Configuration

2.2.4 FPGA Subsystem

The StreetRacer CPU Card includes a Xilinx, SpartanIle, XC2S400-6-FT256 connected to the PXA255 local bus. The FPGA presents a reconfigurable card edge containing 79 dedicated pins and 10 dual purpose pins, to the PXA255. Additional PXA255 peripherals are remapped to the StreetRacer FPGA and FPGA is configuration is under microprocessor control.

2.2.4.1 Clocking

The FPGA has for dedicated clock inputs GCLK_0, GCLK_1, GCLK_2 and GCLK_3. The primary input clock for the FPGA is the PXA255 SDCLK0 which operates approximately 100mHZ. The PXA255 3.6mHZ output clock is provided as an auxiliary input clock. Two additional FPGA clock inputs are available on the card edge.

<i>Clock</i>	<i>Source</i>
GCLK_0	PXA255 3.6mHZ output
GCLK_1	Card edge
GCLK_2	PXA255 SDCLK0
GCLK_3	Card edge

Table 18 FPGA Clock Assignments

2.2.4.2 Local Bus Interface

The FPGA is local bus is connected to PXA255 using the variable latency companion chip interface defined Section 6.9 of the Intel's PXA255 Processor Developers Manual. The FPGA has 32 bit data bus with a 22 bit address bus and uses the PXA255 chips selects nCS1, nCS2, nCS3, nCS4, nCS5. Thus the FPGA presents to the PXA255 5 x 4MB address spaces. The FPGA also has access to the PXA255 DMA request lines DREQ0 and DREQ1.

2.2.4.3 Dual mapped and Remapped PXA255 Peripherals

Several PXA255 peripherals are either directly connected to the FGPA or dual mapped between the FPGA and the card edge. Dual mapped peripherals may be used by the FPGA or the card edge, but not both in the same application board design.

<i>PXA255 Peripheral</i>	<i>Map Type</i>
PCMCIA	Dual Mapped

<i>PXA255 Peripheral</i>	<i>Map Type</i>
PWM	Re-mapped
AC97, I2S	Re-mapped
SSP	Dual Mapped
FFUART	Dual Mapped, CTS, RTS, DCD, DTR, RI, DSR only

Table 19 Peripheral Mapping Assignments

2.2.4.4 Configuration

The FPGA on the StreetRacer CPU Card can be configured via the JTAG interface or under microprocessor control via SelectMap (Slave Parallel Mode). See Xilinx application notes XAPP502 and XAPP176 for more information. In SelectMap program the microprocessor clocks the configuration file into the FPGA via a byte-wide parallel interface.

<i>FPGA Pin</i>	<i>PXA255 Pin</i>
nPROGRAM	GPIO_22
CCLK	GPIO_5
DONE	GPIO_21
D0	GPIO_15
D1	GPIO_78
D2	GPIO_79
D3	GPIO_80
D4	GPIO_33
D5	GPIO_20
D6	GPIO_19
D7	GPIO_28
nINIT	GPIO_29
nCS	GPIO_32
nWRITE	GPIO_30
BUSY	GPIO_31

Table 20 SelectMap Pin Assignments

2.2.5 JTAG Interface

The JTAG interface allows the user to connect to flash programmers, debuggers and boundary scan test systems to the StreetRacer CPU Card. Both the FPGA and the PXA255 are available to the JTAG interface.

Two modes are support, chained and separate. In the chained mode, the PXA255 and

FPGA are connected into a single boundary scan chain and available on header J2. In separate mode the PXA255 and the FPGA are on two difference chains. The PXA255 is available via header J2 and the FPGA is available via header J3. In separate mode, the FGPA can be programmed will the system is running.

<i>Description</i>	<i>Pin</i>	<i>Pin</i>	<i>Description</i>
+3.3V	1	2	GND
TRST	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
GND	11	12	GND
TDO	13	14	GND
RESET_N	15	16	GND
NC	17	18	GND
NC	19	20	GND

Table 21 CPU JTAG Header

<i>Description</i>	<i>Pin</i>
+3.3V	1
GND	2
TCK	3
TDO	4
TDI	5
TMS	6

Table 22 FPGA JTAG Header

2.2.6 LCD Interface

The LCD interface provides access to the PXA255 LCD peripheral. The interface is presented on a low profile 2x16 2mil header J6. See section 7 of Intel's PXA255 Processor Developer's Manual.

<i>Description</i>	<i>Pin</i>	<i>Pin</i>	<i>Description</i>
GND	1	2	+3.3V
L_DD_0	3	4	L_DD_1
L_DD_2	5	6	L_DD_3
L_DD_4	7	8	L_DD_5
L_DD_6	9	10	L_DD_7
L_DD_8	11	12	L_DD_9

<i>Description</i>	<i>Pin</i>	<i>Pin</i>	<i>Description</i>
L_DD_10	13	14	L_DD_11
L_DD_12	15	16	L_DD_13
L_DD_14	17	18	L_DD_15
GND	19	20	GND
L_FCK	21	22	L_LCLK
L_PCLK	23	24	L_BAS
GND	25	26	GND
Reserved	27	28	Reserved
Reserved	29	30	Reserved
GND	31	32	GND

Table 23 LCD Interface Header

2.2.7 Compact Flash Slot

A Compact Flash Slot is provided by the StreetRacer CPU Card. The slot is connected to the PXA255 PCMCIA Slot 0 interface. The slot supports both I/O and memory access modes and is available at physical memory address 0x20000000.

See CompactFlash Associations “CF+ & compact flash Specification Revision 2.1” for detailed information about CF cards. The CF control signals nCD1, nCD2, IREQ and RESET are available of PXA255 GPIO pins.

<i>Signal</i>	<i>PXA255 GPIO</i>
nCD1	GPIO8
nCD2	GPIO9
IREQ	GPIO10
RESET	GPIO6

Table 24 CF Slot GPIO Pins

2.2.8 Bluetooth Serial Interface

The PXA255 BTUART peripheral is available on 2x8 100mill header, J1. The BTUART is connected to the header via a Maxim MAX3225 “1uA Supply Current 1Mbps RS-232 Transceiver with AutoShutdown Plus” and supports baud rates to 921.6Kbps. See section 10 of Intel's “PXA255 Processor Developer's Manual” for more detailed information.

<i>Description</i>	<i>Pin</i>	<i>Pin</i>	<i>Description</i>
BTTXD	1	2	GND
BTRXD	3	4	GND
BTCTS	5	6	GND
BTRTS	7	8	GND

Table 25 BTUART Header

2.2.9 Full Function UART Interface

The PXA255 FFUART is available on the StreetRacer CPU Card edge. The signals FFTXD, FFRXD, FFRTS, and FFCTS are directly mapped to the card edge, while the modem control signals FFDCD, FFDSR, FFRI, and FFDTR are dual mapped to the card edge and the FPGA. These signals may be used by either the FGPA or the card edge but not both. See section 10 of Intel's "PXA255 Processor Developer's Manual" for more detailed information.

The FFUART signals are at logic voltage levels and have not been level shift by a RS-232 transceiver.

<i>Signal</i>	<i>Card Pin</i>
FFTXD	83
FFRXD	168
FFRTS	82
FFCTS	167
FFDCD	164
FFRI	79
FFDSR	80
FFDTR	165

Table 26 FFUART Pin Assignments

2.2.10 Standard UART Interface

The PXA255 STUART peripheral is directly mapped the StreetRacer CPU Card edge. See section 10 of Intel's "PXA255 Processor Developer's Manual" for more detailed information.

The STUART signals are at logic voltage levels and have not been level shift by a RS-232 transceiver.

<i>Signal</i>	<i>Card Pin</i>
IRTXD	69
IRRXD	152

Table 27 STUART Pin Assignments

2.2.11 Synchronous Serial Port

The PXA255 SSP peripheral is dual mapped to the StreetRacer CPU Card edge and the FPGA. These signals may be used by either the FPGA or the card edge but not both. See section 8 of Intel's "PXA255 Processor Developer's Manual" for more detailed information.

<i>Signal</i>	<i>Card Pin</i>
SSPCLK	78
SSPSFRM	161
SSPTXD	76
SSPRXD	160
SSPEXTCLK	78

Table 28 SSP Pin Assignments

2.2.12 Network Synchronous Serial Port

The PXA255 NSSP peripheral is directly mapped to the StreetRacer CPU Card edge. See section 16 of Intel's "PXA255 Processor Developer's Manual" for more detailed information.

<i>Signal</i>	<i>Card Pin</i>
NSSPCLK	157
NSSPSFRM	73
NSSPTXD	75
NSSPRXD	158

Table 29 NSSP Pin Assignments

2.2.13 USB Device Interface

The PXA255 USB Device interface is directly mapped to the StreetRacer CPU Card edge. These pins are bidirectional analog pins with a HiZ reset state. A complete USB interface requires USB transformer, connectors and other glue components. Additionally GPIO access to connector state is recommended. The PXA255 GPIO14 can be used to force the remote USB host to disconnect. A logic one on GPIO14 will force the remote USB host to disconnect. See section 12 of Intel's "PXA255 Processor Developer's Manual" for more detailed information.

<i>Signal</i>	<i>Card Pin</i>
UDCP	155
UDCN	72

Table 30 USB Pin Assignments

2.2.14 AC'97 and I2S Interface

The PXA255 AC'97 and I2S controller are remapped to the FPGA by the StreetRacer CPU Card. The usage of these pins is determined by the application board and the FGPA configuration. The pins may be used as a general purpose I/O interface to the FPGA or the corresponding PXA255 peripheral can be enabled and used. See section 13 and 14 of Intel's "PXA255 Processor Developer's Manual" for more detailed information.

<i>Signal</i>	<i>GPIO</i>
nACRESET	N/A
BITCLK	GPIO28
SDATA_IN0	GPIO29
SDATA_IN1	GPIO32
SYNC	GPIO31
SDATA_OUT	GPIO30

Table 31 I2S GPIO Assignments

2.2.15 Pulse Width Modulator

This PXA255 Pulse Width Modulator remapped to the FPGA by the StreetRacer CPU Card. This usage of these pins is determined by the application board and the FPGA configuration. This pin may be used as general purpose I/O interface to the FPGA or the PWM can be enabled. See section 4.5 of Intel's "PXA255 Processor Developer's Manual" for more detailed information.

With most FPGA configurations supplied by StreetFire Sound Labs, the PWM0 and PWM1 pins are used for FPGA control.

<i>Signal</i>	<i>GPIO</i>	<i>Standard FPGA</i>
PWM0	GPIO16	FPGA_INT
PWM1	GPIO17	nFPGA_RESET

Table 32 PWM GPIO Assignments

2.2.16 Card Edge Definition

The StreetRacer CPU Card edge is designed to be mechanically compatible with all 168 pin DIMM sockets such as Molex's 87609-0059, "DIMM 8-Byte, 168 Circuit" connector. The following table presents the generic StreetRacer CPU Card edge. When mated with a application board new mapped in defined. Always check the application board documentation to find the correct card edge mapping.

<i>Signal</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal</i>
GND	1	85	EB85
EB2	2	86	EB86

<i>Signal</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal</i>
EB3	3	87	EB87
+3.3V	4	88	GND
EB5	5	89	EB89
EB6	6	90	EB90
EB7	7	91	+3.3V
GND	8	92	EB92
EB9	9	93	EB93
EB10	10	94	EB94
EB11	11	95	GND
GND	12	96	EB96
GCK3	13	97	VCC_BANK0
GND	14	98	EB98
EB15	15	99	GND
VCC_BANK7	16	100	EB100
EB17	17	101	EB101
EB18	18	102	+3.3V
GND	19	103	EB103
EB20	20	104	EB104
EB21	21	105	GND
+3.3V	22	106	EB106
EB23	23	107	EB107
EB24	24	108	+3.3V
GND	25	109	EB109
EB26	26	110	EB110
EB27	27	111	GND
+3.3V	28	112	EB112
EB29	29	113	EB113
EB30	30	114	+3.3V
GND	31	115	EB115
EB32	32	116	GND
+3.3V	33	117	EB117
EB34	34	118	GND
GND	35	119	EB119
EB36	36	120	+3.3V
+3.3V	37	121	VCC_BANK7
EB38	38	122	GND

<i>Signal</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal</i>
+3.3V	39	123	EB123
EB40	40	124	EB124
EB41	41	125	+3.3V
GND	42	126	EB126
EB43	43	127	EB127
EB44	44	128	GND
GND	45	129	EB129
EB46	46	130	EB130
EB47	47	131	+3.3V
+3.3V	48	132	EB132
EB49	49	133	EB133
EB50	50	134	GND
GND	51	135	EB135
EB52	52	136	EB136
VCC_BANK6	53	137	VCC_BANK6
EB54	54	138	GND
EB55	55	139	EB139
GND	56	140	EB140
EB57	57	141	EB141
EB58	58	142	+3.3V
EB59	59	143	EB143
+3.3V	60	144	EB144
EB61	61	145	EB145
EB62	62	146	GND
EB63	63	147	GCK1
GND	64	148	nRESET_OUT
GPIO0	65	149	GPIO1
GPIO2	66	150	+3.3V
GPIO3	67	151	GPIO4
GND	68	152	IRRXD/GPIO46
IRTXD/GPIO47	69	153	GND
SCL	70	154	SDA
GND	71	155	UDCP
UDCN	72	156	+3.3V
NSSPSFRM/GPIO82	73	157	NSSPCLK/GPIO81
+3.3V	74	158	NSSPRXD/GPIO84

<i>Signal</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal</i>
NSSPTXD/GPIO83	75	159	GND
SSPTXD/GPIO25	76	160	SSPRXD/GPIO26
GND	77	161	SSPSFRM/GPIO24
SSPEXTCLK/GPIO27	78	162	SSPSCLK/GPIO23
FFRI/GPIO38	79	163	+3.3V
FFDSR/GPIO37	80	164	FFDCD/GPIO36
+3.3V	81	165	FFDTR/GPIO40
FFRTS/GPIO41	82	166	GND
FFTXD/GPIO39	83	167	FFCTS/GPIO35
GND	84	168	FFRXD/GPIO26

Table 33 CPU Card Edge Definition

3 Hardware Programming Guide

This section describes how to configure the RBX1600 memory subsystem and provides detailed programming information for the RBX1600 FPGA Companion Chip peripheral block. Programming information related to PXA255 based peripherals see Intel's "PXA255 Processor Developer's Manual".

3.1 Boot Sequence

Shortly after the application of power through the power jack J1 on the RBX1600 Application Board, or a hardware reset via the switch SW1 on the StreetRacer CPU Card the PXA255 automatically jumps to the reset vector 0x00000000. On the RBX1600 this is the first address in the Flash memory block.

3.2 PXA255 Clock and Power Management Setup

Shortly after the PXA255 jumps to the reset vector the PXA255 the Clock and Power Management Unit of the PXA255 must be configured. This programs the required core oscillators and enables the clock to the integrated peripherals. See Section 3 of the Intel's "PXA255 Processor Developer's Manual" for additional information about these values.

<i>Register Name</i>	<i>Address</i>	<i>Value</i>
CCCR	0x41300000	0x00000161
CKEN	0x41300004	0x000041EF
PSSR	0x40F00004	0x00000030

Table 34 Clock and Power Management Boot Value

3.3 PXA255 System Integration Unit Setup

The RBX1600 uses a variety of resources from the PXA255 and the on-board FPGA, including dual mapped resources and general purpose I/O pins. Shortly after the PXA255 jumps to the reset vector the PXA255 System Integration Unit must be configured.

Table 35 provides a minimum configuration for early boot-stage operation of the RBX1600. Most importantly the PXA255 BTUART and the FFUART are enabled. Of course as the system is booted, additional changes are made to the configuration. See Section 4 of the Intel's "PXA255 Processor Developer's Manual" for additional information about these values.

<i>Register Name</i>	<i>Address</i>	<i>Value</i>
ICMR	0x40d00004	0x00000000
GPSR0	0x40E00018	0x00428820
GPSR1	0x40E0001C	0x00FF0882
GPSR2	0x40E00020	0x0001C000
GPCR0	0x40E00024	0x00000000
GPCR1	0x40E00028	0x00000000
GPCR2	0x40E0002C	0x00000000
GPDR0	0x40E0000C	0x00428860
GPDR1	0x40E00010	0x00FF2A82
GPDR2	0x40E00014	0x0001C000
GAFR0_L	0x40E00054	TBD
GAFR0_U	0x40E00058	TBD
GAFR1_L	0x40E0005C	TBD
GAFR1_U	0x40E00060	TBD
GAFR2_L	0x40E00064	TBD
GAFR2_U	0x40E00068	TBD

Table 35 System Integration Unit Boot Values

3.4 PXA255 Memory Controller Setup

The RBX1600 system is configured with 64MB of 32 bit wide SDRAM located at physical address 0xA0000000, and 64MB of 32 bit wide Flash located at 0x00000000. The StreetRacer CPU Card FPGA Companion Chip is located in 126MB of physical memory starting at 0x10000000. The CF slot is located at physical address 0x20000000.

<i>Chips Select</i>	<i>Address</i>	<i>Usage</i>
nSDCS_0	0xA0000000	SDRAM Bank 0
nCS0	0x00000000	Static Memory Bank 0, Flash
nCS4	0x10000000	Static Memory Bank 4, FPGA Companion Chip
nCS5	0x14000000	Static Memory Bank 5, FPGA Companion Chip

Table 36 CPU Chip Select Assignments

Shortly after the PXA255 jumps to the reset vector and before SDRAM is accessed the PXA255 memory controller must be configured. The values in Table 37 will allow the RBX1600 to access the SDRAM bank and the FPGA Companion Chip. Please be aware that in the case of a power-on reset. The FPGA will not be configured and any accesses will hang the RBX1600. See Section 6 of the Intel's "PXA255 Processor Developer's Manual" for additional information about these values.

<i>Register Name</i>	<i>Address</i>	<i>Value</i>
MDCNFG	0x48000000	0x000008C9
MDMRS	0x48000040	0x01020022
MDREFR	0x48000004	0x0001B017
MSC0	0x48000008	0x74442BD0
MSC1	0x4800000C	0x74447444
MSC2	0x48000010	0x74447444
MECR	0x48000014	0x00000002
MCMEM0	0x48000028	0x00010504
MCMEM1	0x4800002C	0x00010504
MCATT0	0x48000030	0x00010504
MCATT1	0x48000034	0x00010504
MCIO0	0x48000038	0x00010504
MCIO1	0x4800003C	0x00010504

Table 37 Memory Controller Boot Values

3.5 RBX1600 Companion Chip

The RBX1600 FPGA configuration implements a companion chip design which uses a variable latency I/O connection with the PXA255 via the StreetRacer CPU Card local bus. See section 6.9 of Intel's "PXA255 Processor Developer's Manual" for additional information.

The companion chip design implements a reusable infrastructure of Peripheral Blocks (PB). Each peripheral block has the following features:

- All PB's share a common clock derived from the PXA255 SDCLK_0 signal.
- Each PB is individually enabled.
- Each PB has an individual interrupt signal which multiplex onto a single PXA255 GPIO16.

Read or writing to unassigned addresses within the Companion Chip address space is undefined and may hang the system, forcing the user to perform a hardware reset. Reading from reserved bits in the Companion Chip registers will return 0 and writing to reserved bits will be ignored.

<<INSERT COMPANION CHIP BLOCK DIAGRAM>>

3.5.1 Configuration Peripheral Block (CPB)

The Configuration Peripheral Block allows the user to determine the version number of the FPGA design to determine which additional Peripheral Block are configured and enabled. The CPB is assigned to PB0.

3.5.1.1 FPGA Version Register (VERSION)

The VERSION is a read-only register which return the FPGA design version number.

<i>VERSION 0x10000000 (Read-Only)</i>																																
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
VER_NUM																																
Bits	Name		Description																													
32-0	VER_NUM		32 Bit FPGA design version number																													

3.5.1.2 Peripheral Block Capability Register (PBCAP)

The PBCAP is a read-only register which returns a 32 bit field indicating which peripheral blocks are configured in the FPGA design.

<i>PBCAP 0x10000004 (Read-Only)</i>																																
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
PBCAPP																																
Bits	Name		Description																													
32-0	PBCAPP		A 1 in the corresponding bit indicates that the peripheral block is configured. 0 indicates the the peripheral block is not configured.																													

3.5.1.3 Peripheral Block Enable Register (PBEN)

The PBEN register allows the user to specify which peripheral blocks should be enabled. The corresponding bits in this register enable the internal peripheral block clocks and bring the peripheral out of the hardware reset state.

<i>PBEN 0x10000008</i>																																
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
ENABLE																																
Bits	Name		Description																													
32-0	ENABLE		Writing a 1 a particular bit enables the corresponding peripheral block.																													

3.5.2 Interrupt Controller Peripheral Block (ICPB)

The ICPB provides a simple interrupt controller for the all FPGA peripheral block. The ICPB multiplexes 32 PB interrupts onto the PXA255 GPIO16. GPIO16 is active high. Each PB interrupted is latched before being or'ed onto GPIO16. An PB interrupt can be individually enable and disable as well as masked. All PB interrupts must be acknowledged by writing a clear register. The pre-latched PB interrupts are also available. The ICPB is assigned to PB1.

3.5.2.1 Interrupt Status Register (ISTATUS)

The ISTATUS is a read-only register which returns a bit field indicating which PB have generated an interrupt.

<i>ISTATUS 0x10040000 (Read-Only)</i>																																
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
PBSTAT																																
Bits	Name											Description																				
32-0	PBSTAT											A 1 in the corresponding bit indicates that the peripheral block has generated an interrupt.																				

3.5.2.2 Interrupt Mask Register (IMASK)

The IMASK register determines if a PB interrupt will be OR'ed into the ICPB interrupt output. An enabled but masked PB interrupt will still be viable in the ISTATUS and IPENDING registers.

<i>IMASK 0x10040004</i>																																
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
PBMASK																																
Bits	Name											Description																				
32-0	PBMASK											Writing a 1 a particular bit unmask the corresponding peripheral block interrupt.																				

3.5.2.3 Interrupt Enable Register (IENABLE)

The IENABLE register determines if a PB interrupt will be latched into the ISTATUS on the rising edge. A disable PB interrupt will not be visible in the ISTATUS register; it will be visible in the IPENDING register <<CHECK THIS>>. A enabled but masked PB interrupt will not generate an interrupt condition on the ICPB output signal.

<i>IENABLE 0x10040008</i>																																
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
PBENABLE																																
Bits	Name											Description																				
32-0	PBENABLE											Writing a 1 a particular bit enables the corresponding peripheral block interrupt to be latched into the STATUS register.																				

3.5.2.4 Interrupt Clear Register (ICLEAR)

The ICLEAR register is a write-only register used to acknowledged a PB interrupt. Writing a 1 to a particular bit in the register clears the corresponding bit in the ISTATUS register.

<i>ICLEAR 0x1004000C (Write-Only)</i>																															
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
PBCLEAR																															
Bits	Name		Description																												
32-0	PBCLEAR		Writing a 1 a particular bit clears the corresponding peripheral block interrupt latched into the ISTATUS register.																												

3.5.2.5 Interrupt Pending Register (IPENDING)

The IPENDING is a read-only register which returns the raw PB interrupt status before it is latched into the ISTATUS register. This information is available regardless of the state of the ISTATUS and IMASK registers <<CHECK THIS>>.

<i>IPENDING 0x10040010 (Read-Only)</i>																															
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
PBPEND																															
Bits	Name		Description																												
32-0	PBPEND		A 1 in the corresponding bit indicates that the peripheral block is in a interrupt state.																												

3.5.3 SLINK Peripheral Block (SLPB)

The SLPB provides an 8 channel, pulse-width modulator/detector (PWMD) designed to handle Sony's SLINK protocols: CONTROL-AI/II, CONTROL-S, and IR.

Each channel is backed by two 128 byte FIFOs; one transmit and one receive. The timebase used the the PWMD if 100 microseconds and the bit separator is 600 microseconds. To send a SLINK message the software write a series of low pulse-width counts. The PWMD drives the selected line low for the specified time and then releases the line for the bit separator time. This is repeated until the FIFO is empty. To receive a message the PWMD monitors the line for high to low transitions and record the number of time units the receive line is low. This count is added the the receive FIFO. Errors are detected by looking for invalid bit separators. The PWMD detects end of message by monitoring the receive line for idle or high durations of greater than 2 bit separators.

The SLPB can be driven in polled or interrupt mode and support a complete set of status and indicator for managing the internal FIFOs.

3.5.3.1 SLINK Status Register A (SLSTATA)

The SLSTATA is a read-only register containing latched channel status information. These bits are used to generate SLPB interrupts. To clear this bit the SLCLEARA register must be written to.

SLSTATA 0x10080000 (Read-Only)																																
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0
STAT_TS								STAT_RS								STAT_TC								STAT_LI								
Bits	Name											Description																				
31-24	STAT_TS											1 if the corresponding transmitter FIFO is about to run empty.																				
23-16	STAT_RS											1 if the corresponding receiver FIFO is all most full.																				
15-8	STAT_TC											1 if the corresponding transmitter has detected a collision.																				
7-0	STAT_LI											1 if the corresponding receiver line has gone idle.																				

3.5.3.2 SLINK Status Register B (SLSTATB)

The SLSTATB is a read-only register contained channel status information. These bits are unlatched and can not generate a SLPB interrupt.

SLSTATB 0x10080004 (Read-Only)																																
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0
STAT_RO								STAT_TF								STAT_RE								STAT_PLI								
Bits	Name											Description																				
31-24	STAT_RO											1 if the corresponding receiver FIFO has been overrun.																				
23-16	STAT_TF											1 if the corresponding transmitter FIFO is full																				
15-8	STAT_RE											1 if the corresponding received FIFO is empty.																				
7-0	STAT_PLI											1 if the corresponding receiver line is currently idle. This is an unlatched signal.																				

3.5.3.3 SLINK Mask Register A (SLMASKA)

The SLMASKA determines if a particular SLSTATA bit will generate an SLPB interrupt. Regardless of the state of the SLMASKA register SLPB status events will be posted in the SLSTATA register.

SLMASKA 0x10080008																																
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0
MASK_TS								MASK_RS								MASK_TC								MASK_LI								
Bits	Name											Description																				
31-24	MASK_TS											1 enables the corresponding transmitter service interrupt.																				

SLMASKA 0x10080008		
23-16	MASK_RS	1 enables the corresponding receiver service interrupt.
15-8	MASK_TC	1 enables the corresponding transmitter collision interrupt.
7-0	MASK_LI	1 enables the corresponding receive line idle interrupt.

3.5.3.4 SLINK Mask Register B (SLMASKB)

SLMASKB is reserved.

SLMASKB 0x1008000C																																	
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0
RESERVED																																	
Bits	Name		Description																														
32-0	RESERVED																																

3.5.3.5 SLINK Clear Register A (SLCLEARA)

The SLCLEAR is a write-only register which acknowledges the SLPB channel status interrupt. Writing a 1 to a particular bit in the register clears the corresponding bit in the SLSTATA register.

SLCLEARA 0x10080010 (Write-Only)																																	
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0
CLEAR_TS								CLEAR_RS								CLEAR_TC								CLEAR_LI									
Bits	Name		Description																														
31-24	CLEAR_TS		1 clears the corresponding transmitter service interrupt.																														
23-16	CLEAR_RS		1 clears the corresponding receiver service interrupt.																														
15-8	CLEAR_TC		1 clears the corresponding transmitter collision interrupt.																														
7-0	CLEAR_LI		1 clears the corresponding receive line idle interrupt.																														

3.5.3.6 SLINK Clear Register B (SLCLEARB)

SLCLEARB is reserved.

SLCLEARB 0x10080014																																	
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0
RESERVED																																	
Bits	Name		Description																														
32-0	RESERVED																																

3.5.3.7 SLINK Control Register A (SLCNTLA)

The SLCNTLA allows the user to enable/disable the PWM receivers and transmitters as well as clear the receive and transmit FIFOs.

SLCNTLA 0x10080018																															
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0
CLR_TX_FIFO								CLR_RX_FIFO								ENA_TX								ENA_RX							
Bits	Name							Description																							
31-24	CLR_TX_FIFO							Writing a 1 clears the corresponding transmitter FIFO. This bit must be reset to 0 for the FIFO to operate.																							
23-16	CLR_RX_FIFO							Writing a 1 clears the corresponding receiver FIFO. This bit must be reset to 0 for the FIFO to operate.																							
15-8	ENA_TX							1 enables the corresponding transmitter.																							
7-0	ENA_RX							1 enables the corresponding receiver.																							

3.5.3.8 SLINK Control Register B (SLCNTLB)

Reserved.

SLCNTLB 0x1008001C																															
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0
RESERVED																															
Bits	Name							Description																							
32-0	RESERVED																														

3.5.3.9 SLINK Send Register 0-7 (SLSEND[0-7])

Writes to SLSEND registers add a PWM low count to the selected transmit FIFO. SLSTATB can be read to determine the transmit FIFO status.

SLSEND[0-7] 0x10080020 through 0x1008003C																															
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0
RESERVED																SEND_SL															
Bits	Name							Description																							
31-8	RESERVED																														
7-0	SL_SEND							PWM low count to add to the corresponding transmit FIFO.																							

3.5.3.10 SLINK Receive Register 0-7 (SLRCV[0-7])

Reads from the SLRCV registers return the oldest PWM low count in the receive FIFO. SLSTATB can be read to determine the receive FIFO status.

SLRCV[0-7] 0x10080044 through 0x1008005C																															
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
RESERVED																					RCV_SL										
Bits	Name		Description																												
31-8	RESERVED																														
7-0	RCV_SL		PWMD low count to add to the corresponding receive FIFO.																												

3.5.4 Switch Peripheral Block (SWPB)

The SWPB provides access to the RBX1600 Front Panel switch J3. The PB allows the user to check the current state of the switch and setup interrupts for the rise and falling edges of the switch. Switch edge interrupts must be cleared by writing a clear register. The edge interrupts are OR'ed on the PB interrupt signal. The SWPB is assigned to PB3.

3.5.4.1 Switch Status Register (SSTATUS)

The SSTATUS is a read-only register which return the current state of the switch along with indicators for rising and falling edges of the switch.

SSTATUS 0x100C0000 (Read-Only)																															
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
RESERVED																										S	S	S			
																										W	W	W			
																										S	R	F			
																										S	D	D			
Bits	Name		Description																												
32-3	RESERVED																														
2	SWS		0 if the switch is currently pushed, 1 if not.																												
1	SWRD		1 if a switch released event has been detected																												
0	SWFD		1 if a switch pushed event has been detected																												

3.5.4.2 Switch Mask Register (SMASK)

The SMASK determines if a switch edge interrupt will be OR'ed into the PB interrupt output. Regardless of the state of the SMASK register switch edge events will be posted in the SSTATUS register.

SMASK 0x 0x100C0004																															
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0

SMASK 0x 0x100C0004		
RESERVED		S W R M
Bits	Name	Description
32-2	RESERVED	
1	SWRM	Writing a 1 unmaskes the rising edge event and allows it to be OR'ed into the PB interrupt output signal.
0	SWFM	Writing a 1 unmaskes the falling edge event and allows it to be OR'ed into the PB interrupt output signal.

3.5.4.3 Switch Clear Register (SCLEAR)

The SCLEAR is a write-only register which acknowledges the switch edge event interrupt. Writing a 1 to a particular bit in the register clears the corresponding bit in the SSTATUS register.

SCLEAR 0x 0x100C0008 (Write-Only)																																		
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0	S W R C	S W F C
RESERVED																																		
Bits	Name	Description																																
32-2	RESERVED																																	
1	SWRC	Writing a 1 unmaskes the rising edge event and allows it to be OR'ed into the PB interrupt output signal.																																
0	SWFC	Writing a 1 unmaskes the falling edge event and allows it to be OR'ed into the PB interrupt output signal.																																

3.5.5 LED Peripheral Block (LEDPB)

The LEDPB provides access to the RBX1600 Front Panel LED status displays. The LEDPB is assigned to PB5.

3.5.5.1 LED Control Register (LCNTL)

The LCTNL register provides direct access to the Front Panel LED's.

LCNTL 0x10140000																																		
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0		

LCNTL 0x10140000		
RESERVED		LED4 LED3 LED2 LED1 LED0
Bits	Name	Description
32-5	RESERVED	
4	LED4	Set to 1 to light the LED 4
3	LED3	Set to 1 to light the LED 3
2	LED2	Set to 1 to light the LED 2
1	LED1	Set to 1 to light the LED 1
0	LED0	Set to 1 to light the LED 0

3.5.6 Audio Path Control and I2S Peripheral Block (APCIPB)

The APCIPB provide control over the Digital Audio of the RBX1600. The routing interrupt lines of the CS8415A and CS8405A are controlled by the APCIPB. The APCIPB can enable and disable interrupts as well check to interrupt status. Interrupt status must be cleared by access the CS8415A or CS8405A via the SPI bus connected to the NSSP controller of the PXA255. Interrupts must be enabled to cause the APCIPB to OR'ed into the PB interrupt output signal.

The APCIPB also controls the direction of the I2S digital audio bus on the RBX1600. When Digital Audio Input is enabled, the internal I2S shift register provide data to the PXA255 via the I2S port. When disabled the internal I2S shift reads data from the PXA255 I2S port and send the data to the CS8405A and CS4341.

The APCIPB is assigned to PB4.

3.5.6.1 Audio Path Status Register (APSTATUS)

The APSTATUS is a read-only register providing the current interrupt status of the CS8415A and CS8405A. The CS8415A or CS8405A must be accessed to clear the bits in this register.

APSTATUS 0x10100000 (Read-Only)																																	
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0
RESERVED																										C	C	R					
																										S	S	E					
																										8	8	S					
																										4	4	E					
																										0	1	R					
																										5	5	V					
																										AI	AI	E					
																												D					

APSTATUS 0x10100000 (Read-Only)		
Bits	Name	Description
32-4	RESERVED	
3	CS8405AI	1 if the CS8405A has a interrupt condition.
1	CS8415AI	1 if the CS8415A has a interrupt condition.
1-0	RESERVED	1 if a switch pushed event has been detected

3.5.6.2 Audio Path Control Register (APCNTL)

The APCNTL controls the direction of the RBX1600 I2S bus and masks or unmaskes the CS8415A and CS8405A interrupt status. Masked interrupts still appear in the APSTATUS register but do not asset the PB interrupt output signal.

APSTATUS 0x10100000 (Read-Only)																																										
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
RESERVED																												C	C	R	D											
																												S	S	E	A											
																												8	8	S	E											
																												4	4	E	N											
																												0	1	R	A											
																												5	5	V	B											
																												A	A	E	L											
																												M	M	D	E											
Bits	Name	Description																																								
32-4	RESERVED																																									
3	CS8405AM	1 if the CS8405A has a interrupt condition.																																								
2	CS8415AM	1 if the CS8415A has a interrupt condition.																																								
1	RESERVED																																									
0	DAENABLE	1 if the CS8415A is generated the I2S data, 0 if the PXA255 is generating the I2S data.																																								

3.5.7 LAN91C111 Ethernet Controller Interface (ECPB)

The ECPB is a pass-through peripheral block and do not have any internal registers, rather the ECPB bridges the LAN91C111 Ethernet chip onto the StreetRacer CPU Card's local bus. See the LAN91C111 data sheet for detailed programming information.

The LAN91C111 interrupt signal is directly tied to the ECPB interrupt output signal. The PB mapped the LAN91C111 registers to the physical address 0x14000000. The ECPB is assigned to PB16.

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